What is claimed is:

1. An overflow detection circuit comprising:

a plurality of logic elements to receive a group of three most significant bits from sign extended input numbers and to predict three most significant bits of a sum of said input numbers with a carry bit;

said plurality of logic elements to generate an overflow indication for a sum of the input numbers if the predicted three most significant bits has one of a 0 and 1 in the first and second bits respectively and 1 and 0 in the first and second bits respectively for at least one value of the carry bit.

2. The circuit of claim 1, further comprising a final logic element to transmit a 1 from the overflow detection circuit if overflow of the sum is detected and a 0 if overflow of the sum is not detected

3. The circuit of claim 1 wherein said first and second input number are one of mantissas of a floating point number, integers, and carry or sum vectors of numbers in redundant carry-save format.

4. An overflow detection circuit comprising:

A plurality of logic elements to receive at least one bit of a first input number and at least one bit of a second input number wherein a length of said first and second input numbers are extended by one bit;

said plurality of logic elements to receive a group of three most significant bits from

each input number and to predict three most significant bits of a sum of the input numbers with a carry bit;

said plurality of logic elements to generate an overflow indication of a sum of the input numbers if the predicted sum has one of a transition from 0 to 1 in the three most significant bits of the predicted sum and a transition from 1 to in the three most significant bits of the predicted sum for at least one value of the carry bit.

5. The circuit of claim 4, wherein logic elements in a first stage of the overflow circuit are to receive a first bit of each of three most significant bits of each number of extended length, in a second stage of the overflow circuit are to receive a second bit of each of the three most significant bits of each number of extended length, and in a third stage of the overflow circuit are to receive a third bit of each of the three most significant bits of each number of extended length.

6. The circuit of claim 5, wherein the three stages of the overflow circuit are to predict a most significant three bits of the sum of the input numbers for both values 0 and 1 of the carry bit.

7. The circuit of claim 6, wherein the overflow indication is set if two most significant bits of the predicted sum are one of 0 and 1 respectively and 1 and 0 respectively for at least one value of the carry bit.

8. The circuit of claim 7 wherein there are three possible outputs of each stage.

9. The circuit of claim 8, wherein the overflow circuit is implemented using CMOS technology and has at least four stages.

10. The circuit of claim 8, wherein the overflow circuit is implemented using CMOS technology and has fewer than four stages.

11. A method of detecting overflow in addition of two input numbers comprising:

Sign extending the two input numbers;

Receiving at least one bit of a first input number and at least one bit of a second number;

Receiving a group of three most significant bits from each input number;

Predicting three most significant bits of a sum of the input numbers with a carry bit;

Generating an overflow indication of the sum of the input numbers if the predicted sum has one of a 0 and 1 and 1 and 0 in the first and second bits respectively for at least one value of the carry bit.

12. The method of claim 11 wherein said first and second input number are one of mantissas of a floating point number, integers, and carry or sum vectors of numbers in redundant carry-save format.

13. The method of claim 11 further comprising:

Extending a length of said first and second input numbers by one bit.

14. The method of circuit of claim 13, wherein logic elements in a first stage of the overflow circuit are to receive a first bit of each of three most significant bits of each number of extended length, in a second stage of the overflow circuit are to receive a second bit of each of the three most significant bits of each number of extended length, and in a third stage of the overflow circuit are to receive a third bit of each of the three most significant bits of each number of extended length.

15. The method of claim 14, wherein the three stages of the overflow circuit are to predict a most significant three bits of the sum of the input numbers for both carry bit values of 0 and 1.

16. The method of claim 15, wherein the overflow indication is set if two most significant bits of the predicted sum are one of 0 and 1 respectively and 1 and 0 respectively for at least one value of the carry bit.